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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/069,352	WOLRICH ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,14,17,20-25,27-30,33 and 36* is/are rejected.

7)☒ Claim(s) *7,12,13,15,16,18,19,26,31,32,34,35,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/1/07, 7/19/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 5/1/2007 and 7/19/2007, and Amendment as received on 8/1/2007.

Claim Objections

3. Claim 7 is objected to because of the following informalities: It is asked that applicant reword the last paragraph of claim 7 to be more clear. Specifically, it should be made more clear as to what "BP register 2" and "BP register 0" mean. For instance, applicant might prefer to replace the last paragraph with "shifting a second portion of the data into the three least significant bits of a breakpoint (BP) register." This is more clear while still maintaining the desired meaning. Appropriate correction is required.

4. Claim 26 is objected to because of the following informalities: It is asked that applicant reword the last paragraph of claim 26 to be more clear. Specifically, it should be made more clear as to what "BP register 2" and "BP register 0" mean. For instance, applicant might prefer to replace the last paragraph with "shift a second portion of the data into the three least significant bits of a breakpoint (BP) register." This is more clear while still maintaining the desired meaning. Appropriate correction is required.

5. Claims 11 and 30 are objected to because of the following informalities: Applicant uses the following acronyms without first stating what they mean: OV, ADDR, and CTX. Please include the English equivalents in the claim. Appropriate correction is required.

Withdrawn Rejections

6. Applicant, by way of amendment, has overcome the prior art rejections set forth in the previous Office Action for claims 1-38. Consequently, these rejections are hereby withdrawn by the examiner. However, upon further consideration, a new ground(s) of rejection is applied below.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, 6, 8-9, 20-21, 25, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Bhattacharya, U.S. Patent No. 5,704,054.

9. Referring to claim 1, Bhattacharya has taught a method of operating a multi-threaded processor comprising:

a) receiving data specified by execution of a fast-write instruction in one of multiple threads processing on the multi-threaded processor, the one of the multiple threads identified by a processing thread number. See column 6, lines 32-57. Threads, which are inherently identified

by number, and at least also by address in Bhattacharya, also include instructions which specify result data.

b) the fast-write instruction further specifying a register, the register having multiple groups of bits, each group of bits associated with a corresponding thread of the multiple threads processing on the multi-threaded processor. See Fig.6, component 42, and column 6, lines 32-41. Note that a result register, which holds results specified by a "fast-write" instruction, is divided into at least N groups for N threads. Each thread will then write to its portion of the register based on an address identifier.

c) selecting a group of bits associated with the one of the multiple threads, the group of bits being selected from the multiple groups of bits of the register specified by the fast-write instruction according to the processing thread number. Again, see column 6, lines 32-57. When a thread is to write to the result register specified by the fast write, the thread number (address identifier) is used to select the group of bits (portion) to which the result is written.

d) loading the data into the selected bit positions of the register. See column 6, lines 32-57. A thread writes a result to the result register (loads data into the result register).

10. Referring to claim 2, Bhattacharya has taught a method as described in claim 1. Bhattacharya has further taught that the register is a control and status register (CSR). See Fig.6, component 42, and note that a result register, when used as an operand of a dependent instruction, controls that instruction. In addition, it is a status register because writing a result implies completion status of the writing instruction.

11. Referring to claim 6, Bhattacharya has taught a method as described in claim 1. Bhattacharya has further taught that the processing thread represents processing in a micro

engine of a multithreaded processor. See Fig.5, and note a pipeline (micro engine) processes a thread.

12. Referring to claim 8, Bhattacharya has taught a method as described in claim 1. Bhattacharya has further taught that the fast-write instruction comprises a token. See Fig.6 and note the opcode field (OP) in the instruction. This is a token in that this specifies that a particular execution unit is to take control during execution of that instruction.

13. Referring to claim 9, Bhattacharya has taught a method as described in claim 8. Bhattacharya has further taught that the token represents overriding qualifiers. Since the opcode in the instruction contains multiple bits and also specifies that the current contents of a register are to be overwritten with the result of the instruction, the opcode bits may be considered overriding qualifiers, as these bits result in a new result overriding an old result.

14. Referring to claims 20-21, 25, and 27-28, claims 20-21, 25, and 27-28 are rejected for the same reasons set forth in the rejection of claims 1-2, 6, and 8-9, respectively, because Bhattacharya has taught instructions stored on a medium for performing the method of claims 1-2, 6, and 8-9.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3-5, 10-11, 14, 17, 22-24, 29-30, 33, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya.

17. Referring to claim 3, Bhattacharya has taught a method as described in claim 2. Bhattacharya has not explicitly taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. However, as shown in *In re Rose, 105 USPQ 237 (CCPA 1955)*, changes in size are generally not given patentable weight or would have been an obvious improvement. Specifically, the size of Bhattacharya's bus is not disclosed, but a 64-bit bus is a common bus size, which allows for more data to be transported at once than on a 32-bit bus or 16-bit bus, for instance. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bhattacharya's bus to be 64-bits wide. Furthermore, the bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

18. Referring to claim 4, Bhattacharya, as modified, has taught a method as described in claim 3. Furthermore, it is deemed inherent in Bhattacharya that the FIFO bus interfaces with Media Access Controller (MAC) devices. There must be devices that control the means for communicating across a bus (for instance, the buses of Fig.3). These devices are media access controllers as they control media access.

19. Referring to claim 5, Bhattacharya has taught a method as described in claim 1. Bhattacharya has not explicitly taught that the data represents hexadecimal mask values 0 to 0x3FF. However, the examiner asserts that results of a variety of operations may take on any number of values, including those in the range 0 to 0x3FF. The machine would simply have to be at least capable of storing 12-bit results, and storing larger results is well known in the art. A

large result allows for the representation of more values. That is, clearly more values can be represented with 16 bits, for instance, than with 1 bit. Consequently, in order to increase the range of representation of data values, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bhattacharya to include at least a 12-bit result for storing values in the range 0 to 0x3FF.

20. Referring to claim 10, Bhattacharya has taught a method as described in claim 9. Bhattacharya has not explicitly taught that the token is a 32-bit word. However, Bhattacharya has not disclosed the instruction size in any way, and the examiner asserts that 32-bit opcodes are well-known and have been used in the art. The larger the opcode, the more operations that can be encoded. In addition, *In re Rose, 105 USPQ 237 (CCPA 1955)*, changes in size are generally not given patentable weight or would have been an obvious improvement. As a result, in order to encode many operations in Bhattacharya, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bhattacharya's token (opcode) to be a 32-bit word.

21. Referring to claim 11, Bhattacharya, as modified, has taught a method as described in claim 10. Furthermore, Bhattacharya has taught that a token format comprises: an OV field in bit 31, a micro engine (UENG) ADDR field in bits 30:28, a reserved field in bits 27:16, an OV field in bit 15, a fast write data field in bits 14:5, a reserved field in bits 4:3, an OV field in bit 2, and a CTX field in bits 1:0. That is, given Bhattacharya's 32-bit token (resulting from the modification), it can be said that the bits of the token correspond to the above fields as they are merely names, labels, or descriptions of fields, that impart no functionality.

22. Referring to claim 14, Bhattacharya, as modified, has taught a method as described in claim 11. Bhattacharya has further taught that bits 27:16 return 0 when read. That is, in the case where bits 27:16 are set to 0, they will return 0 when read. Note that these bits may all be set to 0 because each bit can take on a 0 or 1 value.

23. Referring to claim 17, Bhattacharya, as modified, has taught a method as described in claim 11. Bhattacharya has further taught that bits 4:3 return 0 when read. That is, in the case where bits 4:3 are set to 0, they will return 0 when read. Note that these bits may all be set to 0 because each bit can take on a 0 or 1 value.

24. Referring to claims 22-24, 29-30, 33, and 36, claims 22-24, 29-30, 33, and 36 are rejected for the same reasons set forth in the rejection of claims 3-5, 10-11, 14, and 17, respectively, because Bhattacharya has taught instructions stored on a medium for performing the method of claims 3-5, 10-11, 14, and 17.

Allowable Subject Matter

25. Claims 7, 12-13, 15-16, 18-19, 26, 31-32, 34-35, and 37-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

26. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection applied above.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hokenek et al., U.S. Patent No. 6,971,103, has taught thread interrupt flag and enable registers which are partitioned into groups of bits for each thread to set such that interrupt related processing is controlled for the individual threads. The examiner would like to point out that while the date of the reference disqualifies it from being applicable prior art, it is being cited since it has taught a similar inventive concept.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
October 2, 2007